CLAIMS

1. An amplifier comprising:

an input terminal to receive an input signal;

a first gain stage comprising a pair of input transistors;

a second gain stage to drive an output stage;

the output stage to provide inverting and non-inverting differential output signals on inverting and non-inverting output nodes; and

a feedback signal electrically connected between the inverting and non-inverting output nodes to emitters of the input transistors through a resistor network.

2. The amplifier of claim 1, the resistor network comprising resistor having values chosen to provide equal gain magnitude to the inverting and non-inverting output nodes from a single-ended input.

3. The amplifier of claim 1, the amplifier further comprising a feedback resistor electrically connected between the inverting node and the input terminal to synthesize an input impedance.

4. The amplifier of claim 1, the input terminal being electrically connected to a ferrite bead.

5. The amplifier of claim 1, the first gain stage further comprising a pair of transistors having emitters electrically connected to the output node through a feedback resistor network.

6. The amplifier of claim 1, the second gain stage further comprising a common emitter amplifier.

7. The amplifier of claim 6, the amplifier further comprising an emitter follower driving the second gain stage.

8. The amplifier of claim 1, the output stage further comprising a constant product loop.

9. The amplifier of claim 1, the output stage further comprising a rail-to-rail output stage.

10. The amplifier of claim 1, the amplifier further comprising a non-linear current source electrically connected to an output transistor on a first side of the amplifier and controlled by the opposite side output signal.

11. An amplifier, comprising:

an input terminal to receive a single input signal;

a first opposite side comprising a non-inverting output node to provide a non-inverting output signal;

a second opposite side comprising an inverting output node to provide an inverting output signal; and

a second gain stage current source biased dynamically dependent upon the opposite side output signal.

12. The amplifier of claim 11, the first stage further comprising a pair of differential transistors having emitters electrically coupled to the high output node through a feedback resistor network.

13. An amplifier, comprising:

an input terminal to receive an input signal;

a first gain stage comprising a pair of input transistors;

an output stage to provide an inverting and non-inverting differential output signals on inverting and non-inverting output nodes; and

a feedback signal electrically connected between the inverting and non-inverting output nodes to emitters of the input transistors through a resistor network.

14. The amplifier of claim 13, the amplifier comprising a second gain stage, wherein the second gain stage drives the output.

15. A selectable-gain amplifier comprising:

an attenuator having an input terminal and a plurality of output terminals, wherein the attenuator is constructed to generate a plurality of output signals at the output terminals responsive to an input signal received an the input terminal; and

a selection stage coupled to the attenuator and arranged to select one of the plurality of output signals responsive to a gain control signal.

16. The amplifier of claim 15 wherein the selection stage comprises a plurality of gm cells.

17. A variable gain amplifier comprising:

an attenuator having a plurality of pairs of tap points; and

a plurality of pairs of gm cells, wherein each pair of gm cells is coupled to a corresponding pair of the tap points.

18. The amplifier of claim 17 wherein each pair of gm cells is constructed and arranged to operate as a multi-tanh cell.

19. An integrated circuit comprising:

a bipolar junction transistor arranged to operate as a saturating switch;

wherein the transistor is dielectrically isolated.